A Fast and an Accurate CORDIC Modulus Extractor Implementation Using FPGA

Mohammed Rizk, Ahmed Hossin, and Alaa Hafez

Abstract—The paper is devoted to design and implement a fast and accurate CORDIC modulus extractor for radar MTD using field programmable gate array FPGA. Modulus extractor receives real and imaginary part from Doppler filter bank and produce a modulus output suitable for amplitude processing by constant false alarm rate processor CFAR. This implementation contributes a fast propagation delay for this extractor and gives an accurate results for the modulus and angle output. This prototype of hardware implementation of CORDIC algorithm used Spartan –III series FPGA, with constraint to area efficiency and throughput architecture. The extractor results show that the conversion time is with less than 0.025% in angle measurement and 0.9% accuracy in modulus measurement which is suitable for real time applications in radar and missile control applications.

Index Terms- MTD, Modulus extractor, CORDIC

1 INTRODUCTION

In the last decade, CORDIC algorithm has drawn wide attention from academia and industry for various applications such as DSP, biomedical signal processing, software defined radio, neural networks, and MIMO systems to mention just a few. It is an iterative algorithm, requiring simple shift and addition operations, for hardware realization of basic elementary functions. Since CORDIC is used as a building block in various single chip solutions, the critical aspects to be considered are high speed, low power, and low area, for achieving reasonable overall performance.

CORDIC algorithm provides an efficient way to estimate the basic elementary functions like trigonometric operations, multiplication, division and some other operations like logarithmic functions, square roots and exponential functions. Most of the applications either in wireless communication or in digital signal processing are based on microprocessors which make use of a single instruction and a bunch of addressing modes for their working. As these processors are costs efficient and offer extreme flexibility but yet are not suited for some of these applications. The CORDIC algorithm has received increased attention after a unified approach is proposed for its implementation [1-2].

The CORDIC arithmetic processor chip is designed and implemented to perform various functions possible in rotation and vectoring mode of circular, linear, and hyperbolic coordinate systems [3]. Since then, CORDIC technique has been used in many applications [4], such as single chip CORDIC processor for DSP applications [5–6]. Recently several researches applied CORDIC algorithm in radar pulse compression, rotary encoders, and waveform generation [7-12]. This paper

2 CORDIC ALGORITHM

The CORDIC algorithm involves rotation of a vector v on the XY-plane in circular, linear and hyperbolic coordinate systems depending on the function to be evaluated. The CORDIC algorithm performs a planar rotation. Graphically, planar rotation means transforming a vector (Xi, Yi) into a new vector (Xj, Yj)[13-14].

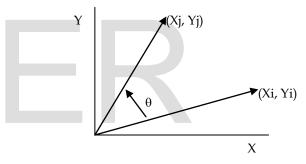


Fig. 1. Rotating the vector

Using a matrix form, a planar rotation for a vector of (Xi, Yi) is defined as

$$\begin{bmatrix} X_{j} \\ Y_{j} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} X_{i} \\ Y_{i} \end{bmatrix}$$
(1)

The \Box angle rotation can be executed in several steps, using an iterative process. Each step completes a small part of the rotation. Many steps will compose one planar rotation. A single step is defined by the following equation:

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \begin{bmatrix} \cos \theta_n & -\sin \theta_n \\ \sin \theta_n & \cos \theta_n \end{bmatrix} \begin{bmatrix} X_n \\ Y_n \end{bmatrix}$$
(2)

Equation 2 can be modified by eliminating the $\cos\theta_n$ factor.

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \cos \theta_n \begin{bmatrix} 1 & -\tan \theta_n \\ \tan \theta_n & 1 \end{bmatrix} \begin{bmatrix} X_n \\ Y_n \end{bmatrix}$$
(3)

Equation 3 requires three multiplies, compared to the four needed in equation 2. Additional multipliers can be eliminated by selecting the angle steps such that the tangent of a step is a International Journal of Scientific & Engineering Research, Volume 5, Issue 3, March-2014 ISSN 2229-5518

(4)

(5)

power of 2. Multiplying or dividing by a power of 2 can be implemented using a simple shift operation. The angle for each step is given by

$$\theta_n = \arctan\left(\frac{1}{2^n}\right)$$

All iteration-angles summed must equal the rotation angle \Box .

 $\sum_{n=0}^{\infty} S_n \theta_n = \theta$

where

$$S_n = \{-1;+1\}\tag{6}$$

This results in the following equation for $\tan \theta_n$

$$\tan \theta_n = S_n 2^{-n} \tag{7}$$

Combining equation 3 and 7 results in

 $\cos \theta_n = \cos \left(\arctan \left(\frac{1}{1} \right) \right)$

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \cos \theta_n \begin{bmatrix} 1 & -S_n 2^{-n} \\ S_n 2^{-n} & 1 \end{bmatrix} \begin{bmatrix} X_n \\ Y_n \end{bmatrix}$$
(8)

Besides for the $\cos\theta_n$ coefficient, the algorithm has been reduced to a few simple shifts and additions. The coefficient can be eliminated by pre-computing the final result. The first step is to rewrite the coefficient.

$$(2^n)$$
 (9)
The second step is to compute equation 9 for all values of
and multiplying the results, which we will refer to as K.

$$K = \frac{1}{P} = \prod_{n=0}^{\infty} \cos\left(\arctan\left(\frac{1}{2^n}\right)\right) \approx 0.607253$$
(10)

K is constant for all initial vectors and for all values of the rotation angle, it is normally referred to as the congregate constant. The derivative P (approx. 1.64676) is defined here because it is also commonly used. We can now formulate the exact calculation the CORDIC performs.

$$\begin{cases} X_{j} = K(X_{i}\cos\theta - Y_{i}\sin\theta) \\ Y_{j} = K(Y_{i}\cos\theta + X_{i}\sin\theta) \end{cases}$$
(11)

Because the coefficient K is pre-computed and taken into account at a later stage, equation 8 may be written as

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \begin{bmatrix} 1 & -S_n 2^{-n} \\ S_n 2^{-n} & 1 \end{bmatrix} \begin{bmatrix} X_n \\ Y_n \end{bmatrix}$$
(12)

or as

$$\begin{cases} X_{n+1} = X_n - S_n 2^{-2n} Y_n \\ Y_{n+1} = Y_n + S_n 2^{-2n} X_n \end{cases}$$
(13)

At this point a new variable called 'Z' is introduced. Z represents the part of the angle \square which has not been totated yet.

$$Z_{n+1} = \theta - \sum_{i=0}^{n} \theta_i \tag{14}$$

For every step of the rotation Sn is computed as a sign of Zn.

$$S_n = \begin{cases} -1 & \text{if } Z_n < 0\\ +1 & \text{if } Z_n \ge 0 \end{cases}$$
(15)

Combining equations 5 and 15 results in a system which reduces the not rotated part of angle \Box tozero. Or in a program-like style:

For n=0 to [inf] If $(Z(n) \ge 0)$ then $Z(n + 1) := Z(n) - atan(1/2^n);$ Else $Z(n + 1) := Z(n) + atan(1/2^n);$

End for;

End if:

The $atan(1/2^{i})$ is pre-calculated and stored in a table. [inf] is replaced with the required number of iterations, which is about 1 iteration per bit (16 iterations yield a 16bit result). If we add the computation for X and Y we get the programlike style for the CORDIC core.

For n=0 to [inf]
If
$$(Z(n) \ge 0)$$
 then
 $X(n + 1) := X(n) - (Yn/2^n);$
 $Y(n + 1) := Y(n) + (Xn/2^n);$
 $Z(n + 1) := Z(n) - atan(1/2^n);$
Else
 $X(n + 1) := X(n) + (Yn/2^n);$
 $Y(n + 1) := Y(n) - (Xn/2^n);$
 $Z(n + 1) := Z(n) + atan(1/2^n);$

End if;

End for;

''n

This algorithm is commonly referred to as driving Z to zero. The CORDIC core computes:

 $[X_{i}, Y_{j}, Z_{j}] = [P(X_{i} \cos(Z_{i}) - Y_{i} \sin(Z_{i})), P(Y_{i} \cos(Z_{i}) + X_{i} \sin(Z_{i})), 0]_{\text{Th}}$

1

$$X_{i} = \frac{1}{P} = K \approx 0.60725$$
$$Y_{i} = 0$$
$$Z_{i} = \theta$$
$$[X_{j}, Y_{j}, Z_{j}] = [\cos\theta, \sin\theta, 0]$$

Another scheme which is possible is driving Y to zero. The CORDIC core then computes:

$$\left[X_{j}, Y_{j}, Z_{j}\right] = \left[P\sqrt{X_{i}^{2} + Y_{i}^{2}}, 0, Z_{i} + \arctan\left(\frac{Y_{i}}{X_{i}}\right)\right]$$

For this scheme there are two special cases:

$$X_i = X$$

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$$Y_{i} = Y$$

$$Z_{i} = 0$$

$$\left[X_{j}, Y_{j}, Z_{j}\right] = \left[P\sqrt{X_{i}^{2} + Y_{i}^{2}}, 0, \arctan\left(\frac{Y_{i}}{X_{i}}\right)\right]$$

$$X_{i} = 1$$

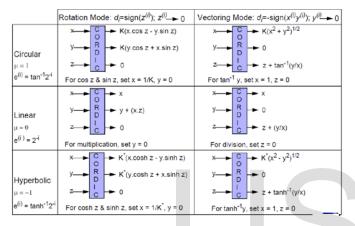
$$Y_{i} = a$$

$$Z_{i} = 0$$

$$\left[X_{j}, Y_{j}, Z_{j}\right] = \left[P\sqrt{1 + a^{2}}, 0, \arctan(a)\right]$$

2

As a Summary of CORDIC Functions is illustrated in table (1) Table (1): Summary of CORDIC Algorithm



3 THE PROPOSED ARCHITECTURE

The MTD is an enhanced configuration of moving-target indicator (MTI) that combines a series of features to improve clutter rejection and target detection. The main features in an MTD are the MTI precanceler, the doppler filter bank, use of burstto-burst PRF diversity, adaptive thresholding, and the clutter map as shown in Fig. 2.

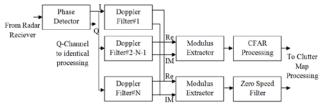


Fig. 2: MTD system block diagram

The doppler filter bank is typically based on the FFT algorithm, providing the following advantages over a delayline canceler: (1) the signal-to-noise ratio is improved by coherent integration within each of the n filters, whose bandwidth will be 1/n that of the canceler; (2) doppler frequency measurement is available, based on the filter number in which detection occurs; (3) the filter bandwidth can be adjusted by amplitude or frequency weighting (windowing), giving better range sidelobe reduction; (4) adaptive thresholding can be applied to each filter, permitting rejection of moving clutter. The adaptive thresholding applies separate thresholds to each filter: the nonzero velocity channels use a range-cell-averaging CFAR to adapt to moving clouds of precipitation, while the zero-velocity channel threshold is generated by the clutter map, which applies a separate threshold for each range cell. In the zero-velocity channel, , targets at zero radial velocity and at the blind speeds can be detected if they exceed by a sufficient margin the clutter stored in the map. The MTD is essentially a low-PRF pulsed doppler processor. Modulus extractor receives real and imaginary part from Doppler filter bank and produces a modulus output suitable for amplitude processing by constant false alarm rate processor CFAR.

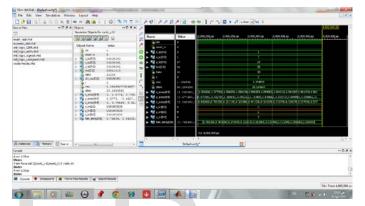


Fig. 3. VHDL simulation of the CORDIC at 30 degree

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Fig. 4. VHDL simulation of the CORDIC at 60 degree



Fig. 5. CORDIC FPGA Implementation

The CORDIC algorithm is implemented into the FPGA to produce modulus output and the angle. The VHDL simulation is demonstrated in Fig. 3-4. The FPGA implementation shown in Fig. 5. Fig. 6. shows CORDIC measured compared with calculated angle concluded the measurement accuracy of the angle. Measured compared with calculated modulus data shown in Fig. 7. Angle Measurement error and Modulus output Measurement error are demonstrated in Fig. 7,8. Angle Measurement error percentage shown in Fig. 9. With maximum error of 0.025%. Fig. 11. Shows Modulus output Measurement error Percentage wit maximum error of 0.9%.

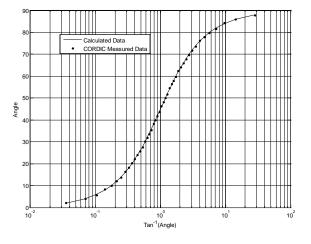


Fig. 6. CORDIC measured compared with calculated angle

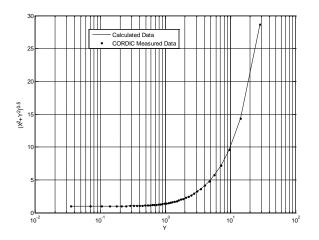


Fig. 7. Measured compared with calculated modulus data

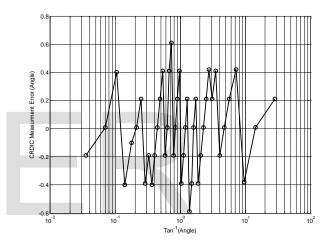


Fig. 8. Angle Measurement error

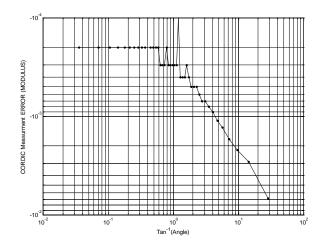


Fig. 9. Modulus output Measurement error

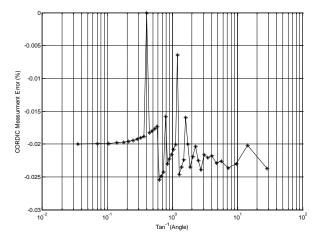


Fig. 10. Angle Measurement error percentage

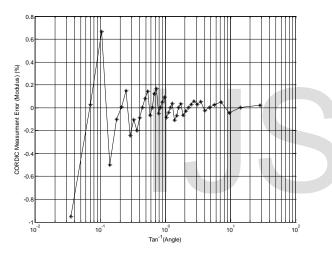


Fig. 11. Modulus output Measurement error Percentage

4 CONCLUSION

This paper design and implement a fast and accurate CORDIC modulus extractor for radar MTD using field programmable gate array FPGA. This implementation contributes a fast propagation delay for this extractor and gives an accurate results for the modulus and angle output. This prototype of hardware implementation of CORDIC algorithm used Spartan –III series FPGA, with constraint to area efficiency and throughput architecture. The extractor results show that the conversion time is less than 1µs with less than 0.025% in angle measurement and 0.9% accuracy in modulus measurement which is suitable for real time applications in radar and missile control applications.

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